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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,541	10/18/2004	Makoto Koshimizu	XA-10191	6425

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EXAMINER	
LEE, KYOUNG	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/511,541	KOSHIMIZU ET AL.	
	Examiner	Art Unit	
	Kyoung Lee	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *1-27* is/are withdrawn from consideration.

5)☒ Claim(s) *38-40* is/are allowed.

6)☒ Claim(s) *28-35 and 37* is/are rejected.

7)☒ Claim(s) *36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/18/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 28-40 in the reply filed on 2/24/2006 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 112

Claim 30 31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 30 recites the limitation "said semiconductor film in said seventh insulation film" in lines 5-6. There is insufficient antecedent basis for this limitation in the claim.

Claim 31 depends from claim 30, it is rejected for the same reason.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 28-31, and 33 rejected under 35 U.S.C. 103(a) as being unpatentable over Klose et al. (U.S. Patent No. 5,326,718).

In re claim 28, Klose disclose a manufacturing method for a semiconductor device, comprising the steps of:

(a) forming a first semiconductor region (33) of a first conductivity type (n-doped) over a semiconductor substrate (31) (see figure 10 and column 7, lines 1-6);

(b) depositing a first insulation film (36) over a main surface of said semiconductor substrate (31) (see figure 10 and column 7, lines 14-20);

(c) depositing a first semiconductor film (37) of a second conductivity type (p-doped) opposite to said first conductivity type (n-dope) over said first insulation film (36);

(d) depositing a third insulation film (39) of a kind different from said first insulation film (36) over said first semiconductor film (37) (see figures 11-12 and column 7, lines 21-31);

(e) depositing a fifth insulation film (310) capable of taking an etching selective ratio to said third insulation film (39) over said third insulation film (39) (see figure 12 and column 7 line 30-33);

(f) opening portions (311) of said fifth insulation film (310) and third insulation film (39) by an etching method using a photoresist film as an etching mask (see figure 13 and column 7, lines 32-51);

(g) removing said photoresist film, and thereafter removing said first semiconductor film (37) exposed from the opening by using said fifth insulation film

(310) as an etching mask to form a first opening portion in said third (39) and fifth insulation films (310) and said first semiconductor film (37) (see figure 14);

(h) forming a sixth insulation film (3131) of a kind different from said first insulation film (36) over a side surface of said first opening portion (311) (see figures 15-16 and column 7, lines 62-68);

(i) forming, over said first insulation film (36), a second opening portion in which a surface opposite to the main surface of said semiconductor substrate and said first semiconductor region (33) in said first semiconductor film (37) are exposed, by selectively etching a portion of said first insulation film (36) through said first opening portion using said third insulation film (39) and sixth insulation film (3131) as etching masks (see figure 16 and column 7 line 62 through column 8 line 9); and

(j) forming a semiconductor film (315) in said second opening portion,

Wherein, during a processing for forming said first opening portion (311), an amount in which a portion of said first insulation film (36) exposed from said first opening portion (311) is etched and a protrusion amount of said sixth insulation film (3131) protruding from a surface opposite to the main surface of said semiconductor substrate (31) toward the main surface of said semiconductor substrate (31) in said first semiconductor film (37) are each set to be equal to or smaller than one half of thickness of said first insulation film (36) (see figures 10-17 and column 7 line 1 through column 8 line 43). The third insulation film (39) is silicon dioxide and the first insulation film (36) is an oxide layer thermally grown at the surface of the single-crystal silicon layer and the examiner consider that the third insulation film is different kind from first insulation film

because an oxide layer thermally grown at the surface of the single-crystal silicon layer does not function same as silicon dioxide. The examiner consider that sixth insulation film (3131) is protruding toward the main surface of first insulation film are each set to be equal to or smaller than one half of thickness of first insulation film (36) since the depth of the etched first insulation film (36) during a process of forming first opening (311) depends on duration of etching.

In re claim 29, Klose disclose the manufacturing method for a semiconductor device further comprising the steps of:

(k) depositing a seventh insulation film (316) over the main surface of said semiconductor substrate after said step (j) (see figure 18); and

(l) forming a fifth semiconductor film (3171) of the first conductivity type via said sixth (3131) and seventh insulation films (316) over the side surface of said first opening portion by a dry-etching method (see figure18-19 and column 8 lines 36-53).

In re claim 30, Klose disclose Klose disclose the manufacturing method for a semiconductor device further comprising:

(m) removing, by the wet-etching method, said seventh insulation film (316) exposed from said fifth semiconductor film (317) in said first opening portion after the step (l), and forming a third opening portion from which a portion of said semiconductor film (315) in said seventh insulation film (316) is exposed (see figure19 and column 8, lines 51-56); and

(n) forming a sixth semiconductor film (318 or 3181) contacting with said semiconductor film and insulated from said first semiconductor film after said step (m) (see figure 19 and column 8 line 53 through column 9 line 13).

In re claim 31, Klose disclose the method wherein said first semiconductor region (33) is a collector region of a bipolar transistor, said first semiconductor film (37) is a base electrode of said bipolar transistor, and said sixth semiconductor film (3181) is an emitter electrode of said bipolar transistor (see figure 20 and column 9 lines 14-30).

In re claim 33, Klose disclose the method wherein said semiconductor film (315, n-doped) is made from a material containing primarily a semiconductor of a kind different from said semiconductor substrate (31, p-doped) (see column 7 lines 1-3 and column 8 lines 29-33).

Claims 32, 34-35, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Klose" in view of Frei et al. (U.S. Patent No. 6,509,242).

In re claim 32, Klose disclose the method as claimed and rejected in claim 28, but Klose does not teach the method wherein said first and fifth insulation films are made from silicon oxide films and said third insulation film and sixth insulation film are made from silicon nitride films. Frei disclose the method wherein said first (17) and fifth insulation (90) films are made from silicon oxide films and said third insulation film (88) and sixth insulation film (100) are made from silicon nitride films (see figure 4F and column 6 lines 18-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to the method wherein said first and fifth insulation

films are made from silicon oxide films and said third insulation film and sixth insulation film are made from silicon nitride films in the method of Klose in order to improve etch selectivity.

In re claim 34, Klose disclose the method as claimed and rejected in claim 33, but Klose does not teach the method wherein said semiconductor film is made from a material containing primarily silicon-germanium. Frei disclose the method wherein said semiconductor film (12) is made from a material containing primarily silicon-germanium (see figure 4H and column 7 lines 11-15). It would have been obvious to one of ordinary skill in the art at the time the invention was made to the semiconductor film made from a material containing primarily silicon-germanium in the method of Klose in order to form the base of the transistor and the resulting transistor can switch faster and yield higher performance and higher frequency.

In re claim 35, Klose disclose the method as claimed and rejected in claim 28, but Klose does not teach the method wherein said semiconductor film is formed by joining a second semiconductor film growing from a surface exposed from said second opening portion of said first semiconductor film and a third semiconductor film growing from the main surface of said semiconductor substrate. Frei disclose the method wherein said semiconductor film is formed by joining a second semiconductor film (13) growing from a surface exposed from said second opening portion of said first semiconductor film and a third semiconductor film (12) growing from the main surface of said semiconductor substrate (see figure 4H and column 7 lines 11-19). It would have been obvious to one of ordinary skill in the art at the time the invention was made to the

semiconductor film formed by joining a second semiconductor film growing from a surface exposed from second opening portion of first semiconductor film and a third semiconductor film growing from the main surface of semiconductor substrate in the method of Klose in order to form the dissimilar crystalline layer.

In re claim 37, Klose disclose the method as claimed and rejected in claim 28, but Klose does not teach the method wherein said fifth insulation film is made from an insulative material of the same kind as said first insulation film. Frei disclose the method wherein said fifth insulation film (90) is made from an insulative material of the same kind as said first insulation film (17) (see column 6 lines 16-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to the fifth insulation film made from an insulative material of the same kind as first insulation film in the method of Klose in order to improve etch selectivity.

Allowable Subject Matter

Claims 38-40 are allowed.

Claim 36 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

Claim 36 recite, "second semiconductor film is a poly crystal and said third semiconductor film is a single crystal".

Claim 38 recite, "forming, in said second opening portion, a second polycrystalline semiconductor film growing from a surface exposed from said second opening portion of said first semiconductor film and forming a link base of said bipolar transistor and a third single crystalline semiconductor film growing from the main surface of said semiconductor substrate and forming a true base region and emitter region of said bipolar transistor, by an epitaxial growth method so that they are joined to each other". The prior art, either singly or in combination, fails to anticipate or render obvious.

Claims 39-40 depend from claim 38 so they are allowable for the same reason.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kyoung Lee whose telephone number is (571) 272-1982. The examiner can normally be reached on M-F 8:30AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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HA NGUYEN
PRIMARY EXAMINER